2012 International Workshop on EUV Lithography Panel Discussion

Q1. EUV Insertion – Timing and Device Drivers?

A1. Intel plans for HVM insertion when EUVL Yields and COO will become beneficial.
Intel's Complementary Litho had patterning requirements similar to DRAM Contact Layer.
I expect Logic Complementary and DRAM Con Litho will drive early EUV HVM adoption.

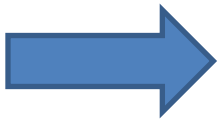
Q2. EUV Insertion - Eco System Requirements?

A2. Scanner: Source >1kW in-band at IF;OL<2nm, Dose<0.5%; Added Print defects $<<10^{-2}/cm^2$
OPC: Fast 3D Mask+Stochastics, Residual model and correction errors <1.5nm max
Resist blur <5nm

Q3. EUV Insertion – Minimal TPT – gradual or full?

A3. Full 100wph or more at Insertion, gradual during Pilot phases

Q4. EUV Scaling Path for 7 and 5nm nodes?

A4. 

Wavelength	13.5	13.5	13.5
NA	0.33	0.33	0.33
Illumination	Parametric	Limited Flex	Free Form
Source Power @IF	1kW	>1.4kW	>1.7kW
Resist blur Sensitivity	<5nm ≥60mj/cm^2	<5nm >60mj/cm^2	<4nm >60mj/cm^2
EUV Exposures/Layer	1	2	2